

FPGA 2007

Fifteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays

Monterey, California
February 18-20, 2007

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Venue: Monterey Beach Resort

The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays is the premier conference for advances in all areas related to FPGAs. Please join us in Monterey, California in February to discuss the latest advances in FPGA architecture, CAD, applications, and technology.

While power reduction has been a recent dominant theme at the conference, the [FPGA 2007 technical program](#) adds two new and interesting emerging themes: **process variation** and **high-performance computing**. As well, a special evening panel debates the merits of high-level languages for FPGA design.

Architecture and CAD papers consider interconnect design with 3D transistor stacking, counting of switch patterns, datapath-oriented architecture synthesis, and power reduction by glitch elimination. Also included are advances in logic design of asynchronous LEs, BDD mapping for power, polarity selection to improve timing, and techmapping using SAT solvers.

Applications papers include security network intrusion detection systems, accelerating ECC cryptosystems, and an ISA for finite field arithmetic, as well as a speech recognition system on FPGAs.

Variation papers include CAD approaches for routing and physical synthesis, using configurations to tolerate within-die (WiD) variation, a study of parametric yield due to WiD, and hardware checkpointing to tolerate faults.

High-performance computing papers include a special **invited session** with speakers from *Xilinx*, *XtremeData*, and *Microsoft Research* on programming FPGAs for computational systems. As well, implementations of a high-performance HyperTransport core, the Pentium CPU design in half of an FPGA, and a PowerPC multiprocessor system on the BEE2 multi-FPGA board are described. Related software advances on multiprocessor system scheduling and microcode compression are also included.

Please visit <http://www.isfpga.org>
Register and Book Hotel by January 19, 2007!

We look forward to seeing you this February at FPGA in Monterey!

Mike Hutton,
Program Chair

André DeHon,
General Chair

Steve Wilton,
Finance Chair

Guy Lemieux,
Publicity Chair

FPGA2007: Preliminary Technical Program

Sunday, February 18

Pre-Conference Workshop on Grand Challenges in FPGA Research	
2:30pm	Session W1: High-level CAD and Architecture
2:40pm to 3:45pm	Jason Cong, <i>UCLA</i>
	Kurt Keutzer, <i>UCB</i>
	Grant Martin, <i>Tensilica</i>
	Discussion
3:45pm	Break
4:10pm	Session W2: Low-level CAD and Architecture
4:15pm to 5:30pm	Vaughn Betz, <i>Altera</i>
	Steve Trimberger, <i>Xilinx</i>
	Jonathan Rose, <i>Toronto</i>
	André DeHon, <i>U.Penn</i>
	Discussion
Reception	
6pm	Registration
7pm	Opening Reception

Monday, February 18

Dinner and Evening Panel	
7:00pm	<i>High-Level Languages for FPGAs – The Future, or a Passing Fad?</i>
	Organizer: Michael Wirthlin , Brigham Young University
	Misha Burich, <i>Altera</i>
	Andrew Guyler, <i>Mentor</i>
	Brian von Herzen, <i>Rapid Prototypes</i>
	Maya Gokhale, <i>Lawrence Livermore</i>
	Glenn Steiner, <i>Xilinx</i>

Monday, February 19

Session 1: Architecture And Technology	
8:40am	Opening Remarks
9:00am	<i>A Routing Fabric for Monolithically Stacked 3D-FPGA</i> Mingjie Lin and Abbas El Gamal, Stanford
	<i>Design of a Logic Element for Implementing an Asynchronous FPGA</i> Scott Smith , University of Missouri – Rolla
	<i>Designing Efficient Input Interconnect Block for LUT Clusters Using Counting and Entropy</i> Wenyi Feng and Sinan Kaptanoglu, Actel
	<i>A Synthesizable Datapath-Oriented Embedded FPGA Fabric</i> Steven Wilton , C.H. Ho, P. Leong, W. Luk and B. Quinton, Imperial College, London and UBC, Canada
10:20am	Poster Session 1
Session 2: Implementation and Emulation	
11:15am	<i>A versatile, low latency HyperTransport core</i> David Slognat , Alexander Giese and Ulrich Bruening, University of Mannheim, Germany
	<i>An FPGA-Based Pentium(R) in a Complete Desktop System</i> Shih-Lien Lu , Peter Yiannacouras, Taeweon Suh, Rolf Kassa, and Michael Konow Intel Corp, University of Toronto, and Georgia Tech.
	<i>A 1000-Word Vocabulary [...] Speech Recognizer Implemented in a Single FPGA</i> Edward Lin , Kai Yu, Rob Rutenbar and Tshuan Chen, CMU
12:15pm	Lunch
Session 3: CAD	
2pm	<i>Variation-Aware Routing for FPGAs</i> Satish Sivaswamy and Kia Bazargan, Univ. of Minnesota
	<i>Stochastic Physical Synthesis [...] with [Interconnect Uncertainty] and Process Variation</i> Yan Lin and Lei He, UCLA
	<i>Post-Route LUT Output Polarity Selection for Timing Optimization</i> Kai Zhu , Actel Corp.
3pm	Poster Session 2
Session 4: FPGA-based Computing	
4pm	<i>Synthesis of an Application-Specific Soft Multiprocessor System</i> Jason Cong, Guoling Han and Wei Jiang, UCLA
	<i>FPGA-friendly Code Compression Technique for Horizontal Microcoded Custom IPs</i> Bita Gorjiara and Daniel Gajski, UC Irvine
	<i>A Practical FPGA-based Framework for Novel CMP Research</i> Sewook Wee, J. Casper, N. Njoroge , Y. Teslyar, D. Ge, C. Kozyrakis, and K. Olukotun, Stanford
Dinner and Evening Panel	
7:00pm	<i>High-Level Languages for FPGAs – The Future, or a Passing Fad?</i> Michael Wirthlin (BYU), Misha Burich (Altera), Andrew Guyler (Mentor), Brian von Herzen (Rapid Prototypes), Maya Gokhale (Lawrence Livermore), Glen Steiner (Xilinx)

Tuesday, February 20

Session 5: Invited Session : Integrating FPGAs in High-Performance Computing	
8:45am	Organizers: <i>Paul Chow (University of Toronto) and Mike Hutton (Altera)</i>
	<i>High-Performance Computing Business Overview and Perspective</i> Dan Gibbons Director, Xilinx Business Development, San Jose, CA, USA
	<i>System, Architecture and Implementation Perspective</i> Nathan Woods Principal Scientist, XtremeData, Schlomberg, IL, USA
	<i>Programming Models for Parallel Systems, the Programmers Perspective</i> Satnam Singh, Microsoft Research, Cambridge, UK
10:10am	Poster Session 3
Session 6: CAD and Architecture	
11:00am	<i>Improved SAT-Based Boolean Matching Using Implicants for LUT-Based FPGAs</i> Kirill Minkovich and Jason Cong, UCLA
	<i>Power-Aware FPGA Logic Synthesis Using Binary Decision Diagrams</i> Kevin Tinmaung and Russell Tessier, University of Massachusetts, Amherst
	<i>GlitchLess: An Active Glitch Minimization Technique for FPGAs</i> Julien Lamoureux, Guy Lemieux and Steven J.E. Wilton, The University of British Columbia, Canada
12pm	Lunch
Session 7: Variation & Yield	
1:30pm	<i>Performance and Yield Enhancement of FPGAs with Within-die Variation using Multiple Configurations</i> Yohei Matsumoto, M. Hioki, T. Kawanami, T. Tsutsumi, T. Nakagawa, T. Sekigawa and H. Koike, AIST, Japan
	<i>Parametric Yield in FPGAs Due to Within-die Delay Variations: A Quantative Analysis</i> Pete Sedcole and Peter Y. K. Cheung, Imperial College London
	<i>Efficient Hardware Checkpointing -- Concepts, Overhead Analysis, and Implementation</i> Dirk Koch, Christian Haubelt and Juergen Teich, University of Erlangen-Nuremberg
2:30pm	Break
Session 8: Security	
2:50pm	<i>The Shunt: An FPGA-Based Accelerator for Network Intrusion Prevention</i> Nicholas Weaver, Vern Paxson and Jose Gonzalez, ICSI Berkeley
	<i>Attacking Elliptic Curve Cryptosystems with Special-Purpose Hardware</i> Tim Güneysu, Christof Paar and Jan Pelzl, University of Bochum, Germany
	<i>Reconfigurable Finite Field Instruction Set Architecture</i> Nathan Jachimiec, Fernando Martinez-Vallina and Jafar Saniie, Illinois Inst. of Technology
3:50pm	Closing Remarks

FPGA 2007 Pre-Conference Workshop on Grand Challenges in FPGA Research

Sunday, February 18, 2:30pm *No registration required!*

Objective

This special pre-conference workshop aims to bring together top researchers from industry and academia to identify some of the most challenging research problems that are facing FPGAs.

This workshop will be particularly useful for up-and-coming young researchers who are beginning their career. Where is the low-hanging fruit, and what problems are worth addressing as academics or as industrial researchers? What types of problems are likely to win funding support? Learn from the advice of our specially invited presenters and from challenges and contributions from the audience!

Presenters

Session W1: High-level CAD and Architecture

- Jason Cong, *UCLA*
- Kurt Keutzer, *UCB*
- Grant Martin, *Tensilica*

Session W2: Low-level CAD and Architecture

- Vaughn Betz, *Altera*
- Steve Trimberger, *Xilinx*
- Jonathan Rose, *Toronto*
- André DeHon, *U.Penn*

Questions

Some of the questions to be pondered are summarized below:

- is FPGA synthesis, place and route mature?
- are current algorithms and tools close to optimal? is there evidence?
- where is there room and need for innovation?
- are the big challenges moving to higher levels (system/high-level synthesis) or lower levels (DFM/DFY/DSM issues, reliability, variation?)
- is dynamic/runtime management of FPGA resources needed?
- where can young researchers expect to make a big impact?
- what challenges/problems, if solved, will bring you community accolades? (and what problems are so well trod they should be approached with care?)
- which is more mature / needs more research: architecture? CAD? both?
- what promises or challenges does nanotechnology deliver to FPGAs?