

## Fourteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays

### Wednesday, February 22

- 6:00PM–8:00PM Registration  
 7:00PM–8:30PM Welcome Reception

### Thursday, February 23

- 8:30AM Continental Breakfast  
 Registration Opens (closes at 4:00PM)  
 Sponsor and Exhibit Hall Opens (closes at 5:00PM)
- 8:45AM Opening and Welcome (Steve Wilton and André DeHon)
- 9:00AM Session 1: Architecture 1 (Chair: Trevor Bauer)
- *A 90nm Low-Power FPGA for Battery-Powered Applications*  
 Tim Tuan, Sean Kao, Arif Rahman, Satyaki Das, and Steve Trimberger  
 Xilinx Inc.
  - *Embedded Floating-Point Units in FPGAs*  
 Michael J. Beauchamp, Scott Hauck, Keith D. Underwood, and K. Scott Hemmert  
 University of Washington
  - *Measuring the Gap Between FPGAs and ASICs*  
 Ian Kuon and Jonathan Rose  
 University of Toronto
- 10:00AM Poster Session 1 (Chair: Eric Sather)
- 11:00AM Session 2: CAD 1 (Chair: Kia Bazargan)
- *Optimality Study of Logic Synthesis for LUT-Based FPGAs*  
 Jason Cong and Kirill Minkovich  
 University of California, Los Angeles
  - *Improvements to Technology Mapping for LUT-Based FPGAs*  
 Alan Mishchenko, Satrajit Chatterjee, and Robert Brayton  
 University of California, Berkeley
  - *Improving Performance and Robustness of Domain-Specific CPLDs*  
 Mark Holland and Scott Hauck  
 University of Washington
- 12:00PM Lunch
- 1:30PM Session 3: Application 1 (Chair: John Wawrzynek)
- *Design, Implementation, and Verification of Active Cache Emulator (ACE)*  
 Jummit Hong, Eriko Nurvitadhi, and Shih-Lien Lu  
 Intel Corp.
  - *Modeling the Data-Dependent Performance of Pattern-Matching Architectures*  
 Christopher R. Clark and David E. Schimmel  
 Georgia Tech
  - *An Iterative Division Algorithm for FPGAs*  
 Jianhua Liu, Michael Chang, and Chung-Kuan Cheng  
 University of California, San Diego
- 2:30PM Poster Session 2 (Chair: Lei He)
- 3:30PM Session 4: Architecture 2 (Session Chair: Carl Ebeling)
- *Yield Enhancements of Design-Specific FPGAs*  
 Nicola Campregher, Peter Y.K. Cheung, George A. Constantinides, and Milan Vasilko  
 Imperial College
  - *FPGA Clock Network Architecture: Flexibility vs. Area and Power*  
 Julien Lamoureux and Steven J.E. Wilton  
 University of British Columbia
- 6:00PM Conference Banquet
- 7:00PM Evening Panel (Moderator: Mike Hutton)  
*Will Power Kill FPGAs?*

**Poster Program for Thursday, February 23**

- 10:00AM Poster Session 1: Architectures (Chair: Eric Sather)
- *FPGAs with multidimensional mesh topology*  
Yohei Matsumoto, Hanpei Koike, and Akira Masaki  
National Institution of Advanced Industrial Science and Technology, Japan
  - *Evaluation of Granularity on Threshold Voltage Control in Flex Power FPGA*  
Masakazu Hioki, Takashi Kawanami, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa and Hanpei Koike  
National Institution of Advanced Industrial Science and Technology, Japan
  - *A Novel Methodology for Designing High-Performance and Low-Energy FPGA Routing Architecture*  
Konstantinos Siozios, Konstantinos Tatas, Dimitrios Soudris, and Antonios Thanailakis Democritus University of Thrace
  - *Autonomous-Repair Cell for Fault Tolerant Dynamic-Reconfigurable Devices*  
Kentaro Nakahara, Shin'ichi Kouyama, Tomonori Izumi, Hiroyuki Ochi, and Yukihiro Nakamura  
Kyoto University
  - *A Programmable Majority Logic Array Using Molecular Scale Electronics*  
Garrett S. Rose and Mircea R. Stan  
University of Virginia
  - *A Multilevel Hierarchical Interconnection Structure for FPGA*  
Hayder Mrabet, Zied Marrakchi, Pierre Souillot, and Habib Mehrez  
ASIM-LIP6
  - *Test and Recovery for Fine-Grained Nanoscale Architectures*  
Mohammad Tehranipoor and Reza M. Rad  
University of Maryland Baltimore County
  - *Fine-Grained Island Style Architecture for Molecular Electronic Devices*  
Reza M. Rad and Mohammad Tehranipoor  
University of Maryland Baltimore County
  - *Post-Placement Interconnect Entropy*  
Wenyi Feng and Jonathan Greene  
Actel Corporation
  - *A Type Architecture for Hybrid Micro-Parallel Computers*  
Benjamin Ylvisaker, Brian Van Essen, and Carl Ebeling  
University of Washington
- 2:30PM Poster Session 2: CAD (Chair: Lei He)
- *Testing Embedded RAM Modules in SRAM-Based FPGAs*  
Mohammed Y Niamat, Dinesh Nemade, Mohsin M Jamali  
University of Toledo
  - *Jaguar: A Compiler Infrastructure for Java Reconfigurable Computing*  
Youngsun Han, Seokjoong Hwang, and Seon Wook Kim  
Korea University
  - *Effective Clustering Technique to Optimize Routability of Outer Cluster Nets*  
Masaki Kobata, Masahiro Iida, and Toshinori Sueyoshi  
Kumamoto University
  - *Configuration tools for a new Multilevel Hierarchical FPGA*  
Marrakchi Zied, Mrabet Hayder, And Mehrez Habib  
ASIM-LIP6
  - *Simulative Analysis of Dynamic Scheduling Heuristics for Reconfigurable Computing of Parallel Applications*  
Rajagopal Subramaniyan, Ian Troxel, Alan D. George, and Melissa Smith  
University of Florida

**Friday, February 24**

- 8:30AM Continental Breakfast  
Registration Opens (closes at 12:00PM)  
Sponsor and Exhibit Hall Opens (closes at 4:00PM)
- 9:00AM Session 5: Emerging Technologies (Chair: Guy Lemieux)
- *Performance Benefits of Monolithically Stacked 3D-FPGA*  
Mingjie Lin, Abbas El Gamal, Yi-Chang Lu, and Simon Wong  
Stanford University
  - *Magnetic Tunneling Junction based FPGA*  
Nicolas Bruchon, Lionel Torres, Gilles Sassatelli, and Gaston Cambon  
LIRMM/UMII
  - *A Reconfigurable Architecture for Hybrid CMOS/Nanodevice Circuits*  
Dmitri B. Strukov and Konstantin K. Likharev  
Stony Brook University
- 10:00AM Poster Session 3 (Chair: Miriam Leeser)
- 11:00AM Session 6: Application 2 (Chair: John Lockwood)
- *A Reconfigurable Hardware Based Embedded Scheduler for Buffered Crossbar Switches*  
Lotfi Mhamdi, Christopher Kachris and Stamatis Vassiliadis  
Delft University of Technology
  - *An Adaptive Reed Solomon Errors-and-Erasures Decoder*  
Lilian Atieno, Jonathan Allen, Dennis Goeckel, and Russell Tessier  
University of Massachusetts
  - *A Compact FPGA Implementation of the Hash Function Whirlpool*  
Norbert Pramstaller, Christian Rechberger, and Vincent Rijmen  
Graz University of Technology
- 12:00PM Lunch  
Registration Closes
- 1:30PM Session 7: CAD 2 (Chair: Katherine Compton)
- *Armada: Timing-Driven Pipeline-Aware Routing for FPGAs*  
Ken Eguro and Scott Hauck  
University of Washington
  - *Combining Module Selection and Resource Sharing for Efficient FPGA Pipeline Synthesis*  
Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer  
Brigham Young University
  - *Power-Aware RAM Mapping for FPGA Embedded Memory Blocks*  
Russell Tessier, Vaughn Betz, David Neto, and Thiagaraja Gopalsamy  
University of Massachusetts
- 2:30PM Break
- 3:30PM Session 8: Application 3 (Chair: Charle' Rupp)
- *Application-Specific Customization of Soft Processor Microarchitecture*  
Peter Yiannacouras, J. Gregory Steffan, and Jonathan Rose  
University of Toronto
  - *Fast and Accurate Resource Estimation of Automatically Generated Custom DFT IP Cores*  
Peter A. Milder, Mohammad Ahmad, James C. Hoe, and Markus Pueschel  
Carnegie Mellon University
- 4:10PM Closing Remarks

**Poster Program for Friday, February 24**

- 10:00AM Poster Session 3: Applications (Chair: Miriam Leeser)
- *High Speed FIR Filter Implementation Using Add and Shift Method*  
Shahnam Mirzaei, Anup Hosangadi, and Ryan Kastner  
University of California at Santa Barbara
  - *Manifold Similarity Search of DNA Sequences with Reconfigurable Hardware*  
Thinh Ngoc Tran, Surin Kittitornkun, and Shigenori Tomiyama  
King Mongkut's Institute of Technology, Ladkrabang
  - *The Routability of Multiprocessor Network Topologies in FPGAs*  
Manuel Saldaña, Lesley Shannon, and Paul Chow  
University of Toronto
  - *FPGA based RAID 6 Hardware Accelerator*  
Michael Gilroy, James Irvine, and William Berrie  
Institute for System Level Integration / A2E
  - *A Real-Time Implementation of Richardson-Lucy Deconvolution*  
Oliver Sims and James Irvine  
Institute for System Level Integration
  - *A Generic Lookup Cache Architecture for Network Processing Applications*  
Janardhan Singaraju and John A Chandy  
University of Connecticut
  - *Efficient use of Communications Between an FPGA's Embedded Processor and its Reconfigurable Logic*  
Joshua Noseworthy and Miriam Leeser  
Mercury Computer Systems
  - *Building a Flexible and Scalable DRAM Interface for Networking Applications on FPGAs*  
Jike Chong, Chidamber Kulkarni, and Gordon Brebner  
University of California at Berkeley
  - *Periodic Licensing of FPGA Based Intellectual Property*  
Nathaniel Couture and Kenneth B. Kent  
University of New Brunswick
  - *A Performance Model for Accelerating Scientific Applications on Reconfigurable Computers*  
Ronald Scrofano and Viktor K Prasanna  
University of Southern California
  - *Reconfigurable Computing with Multiscale Data Fusion for Remote Sensing*  
Vikas Aggarwal, Alan D. George, and Kenneth C Slatton  
University of Florida
  - *A Reconfigurable Architecture for Network Intrusion Detection using Principal Component Analysis*  
David T. Nguyen, Gokhan Memik, and Alok Choudhary  
Northwestern University
  - *GSFAP Adaptive Filtering using Log Arithmetic for Resource-Constrained Embedded Systems*  
Milan Tichy, Andy Nisbet, and David Gregg  
University of Dublin
  - *Flexible Implementation of Genetic Algorithms on FPGAs*  
Tatsuhiko Tachibana, Yoshihiro Murata, Naoki Shibata, Keiichi Yasumoto, and Minoru Ito  
Graduate School of Information Science Nara Institute of Science and Technology
  - *Context-Free-Grammar based Token Tagger in Reconfigurable Devices*  
Young H. Cho, James Moscola, and John W. Lockwood  
Washington University in St. Louis