

FPGA 2006

Fourteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays

Monterey, California
February 22-24, 2006

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CALL FOR PARTICIPATION

Venue: Hyatt Regency Monterey

The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays is the premier conference for presentation of advances in all areas related to FPGA technology. Please join us in Monterey, California to discuss the latest advances in FPGA architecture, CAD, applications, and emerging technology.

This year the conference has an exceptionally exciting program. Architecture papers consider design of a low-power 90nm FPGA, embedding floating-point units, design of clocking networks, the sustainability of defect tolerance, and a quantitative comparison of FPGAs versus ASICs. CAD papers study the optimality and performance of logic synthesis and technology mapping, design for layout, pipeline synthesis, pipelined routing, and power-aware technology mapping into RAMs. Novel applications include a cache emulator, an adaptive reed solomon decoder, an interative division algorithm, a crossbar scheduler, a unified comparison of pattern-matching circuit architectures, customized soft core processors, custom discrete Fourier transform cores, and a secure hash function. Emerging technology papers provide a snapshot of longer-term research that promises to significantly alter FPGAs as we know them: vertically stacking multiple active CMOS transistor layers, mapping circuits to a hybrid CMOS/NANO architecture, and a non-volatile magnetic tunneling junction FPGA.

Visit <http://www.isfpga.org> for further details
(sample web menu options shown on left)

See the Preliminary Program (shown on back)

Key Dates:

Early Registration: January 31, 2006

Hotel Reservations: 5pm PST, February 1, 2006

**André DeHon,
Program Chair**

**Guy Lemieux,
Publicity Chair**

FPGA2006: Preliminary Technical Program

Thursday, February 23

Session 1: Architecture 1	
9:00am	<i>A 90nm Low-Power FPGA for Battery-Powered Applications</i> Tim Tuan, Sean Kao, Arif Rahman, Satyaki Das, and Steve Trimberger Xilinx Inc.
	<i>Embedded Floating-Point Units in FPGAs</i> Michael J. Beauchamp, Scott Hauck, Keith D. Underwood, and K. Scott Hemmert University of Washington
	<i>Measuring the Gap Between FPGAs and ASICs</i> Ian Kuon and Jonathan Rose University of Toronto
10am	Poster Session 1
Session 2: CAD 1 (Chair: Kia Bazargan)	
11:00am	<i>Optimality Study of Logic Synthesis for LUT-Based FPGAs</i> Jason Cong and Kirill Minkovich UCLA
	<i>Improvements to Technology Mapping for LUT-Based FPGAs</i> Alan Mishchenko, Satrajit Chatterjee, and Robert Brayton Improvements to Technology Mapping for LUT-Based FPGAs
	<i>Improving Performance and Robustness of Domain-Specific CPLDs</i> Mark Holland and Scott Hauck University of Washington
12pm	Lunch
Session 3: Application 1 (Chair: John Wawrzynek)	
1:30pm	<i>Design, Implementation, and Verification of Active Cache Emulator (ACE)</i> Jummit Hong, Eriko Nurvitadhi, and Shih-Lien Lu Intel Corp.
	<i>An Adaptive Reed Solomon Errors-and-Erasures Decoder</i> Lilian Atieno, Jonathan Allen, Dennis Goeckel, and Russell Tessier University of Massachusetts
	<i>An Iterative Division Algorithm for FPGAs</i> Jianhua Liu, Michael Chang, Chung-Kuan Cheng University of California, San Diego
2:30pm	Poster Session 2
Session 4: Architecture 2 (Session Chair: Carl Ebeling)	
3:30pm	<i>Yield Enhancements of Design-Specific FPGAs</i> N. Campregher, P.Y.K. Cheung, G.A. Constantinides, and M. Vasilko Imperial College
	<i>FPGA Clock Network Architecture: Flexibility vs. Area and Power</i> Julien Lamoureux and Steven J.E. Wilton University of British Columbia
Evening Panel (Moderator: Mike Hutton)	
7:00pm	TBA

Friday, February 24

Session 5: Emerging Technologies (Chair: Guy Lemieux)	
9:00am	<i>Performance Benefits of Monolithically Stacked 3D-FPGA</i> Mingjie Lin, Abbas El Gamal, Yi-Chang Lu, and Simon Wong Stanford University
	<i>Magnetic Tunneling Junction based FPGA</i> Nicolas Bruchon, Lionel Torres, Gilles Sassatelli, and Gaston Cambon LIRMM/UMII
	<i>A Reconfigurable Architecture for Hybrid CMOS/Nanodevice Circuits</i> Dmitri B. Strukov and Konstantin K. Likharev Stony Brook University
10am	Poster Session 3
Session 6: Application 2 (Chair: John Lockwood)	
11:00am	<i>A Reconfigurable Hardware Based Embedded Scheduler for Buffered Crossbar Switches</i> Lotfi Mhamdi, Christopher Kachris and Stamatis Vassiliadis Delft University of Technology
	<i>Modeling the Data-Dependent Performance of Pattern-Matching Architectures</i> Christopher R. Clark and David E. Schimmel Georgia Tech
	<i>A Compact FPGA Implementation of the Hash Function Whirlpool</i> Norbert Pramstaller, Christian Rechberger, and Vincent Rijmen Graz University of Technology
12pm	Lunch
Session 7: CAD 2 (Chair: Katherine Compton)	
1:30pm	<i>Armada: Timing-Driven Pipeline-Aware Routing for FPGAs</i> Ken Eguro and Scott Hauck University of Washington
	<i>Combining Module Selection and Resource Sharing for Efficient FPGA Pipeline Synthesis</i> Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer Brigham Young University
	<i>Power-Aware RAM Mapping for FPGA Embedded Memory Blocks</i> Russell Tessier, Vaughn Betz, David Neto, and Thiagaraja Gopalsamy University of Massachusetts
2:30pm	Break
Session 8: Application 3 (Chair: Jeff Arnold)	
3:30pm	<i>Application-Specific Customization of Soft Processor Microarchitecture</i> Peter Yiannacouras, J. Gregory Steffan, and Jonathan Rose University of Toronto
	<i>Fast and Accurate Resource Estimation of Automatically Generated Custom DFT IP Cores</i> Peter A. Milder, Mohammad Ahmad, James C. Hoe, and Markus Pueschel Carnegie Mellon University