FPGA 2005
International Symposium on Field-Programmable Gate Arrays
Monterey, California
February 20-22, 2005

Sunday, February 20	
6:00pm-9:00pm	Registration
7:00pm-8:30pm	Welcome Reception

Monday, February 21		
7:00am-5:00pm	Registration	
7:30am-8:15am	Continental Breakfast	
8:00am-5:00pm	Sponsor and Exhibit Room	
8:20am-8:30am	Welcoming Remarks: Herman Schmit, Steve Wilton	
8:30am-9:30am	Session 1: New FPGA Architectures Chair: Carl Ebeling, University of Washington	
	8:30	*Using Bus-Based Connections to Improve Field-Programmable Gate Array Density for Implementing Datapath Circuits* Andy Gean Ye and Jonathan Rose, University of Toronto
	8:50	*The Stratix-II Logic and Routing Architecture* David Lewis, Elias Ahmed, Gregg Baeckler, Vaughn Betz, Mark Bourgeault, David Cashman, David Galloway, Mike Hutton, Chris Lane, Andy Lee, Paul Leventis, Sandy Marquardt, Cameron McClintock, Ketan Padalia, Bruce Pedersen, Giles Powell, Boris Ratchev, Srinivas Reddy, Jay Schleicher, Kevin Stevens, Richard Yuan, Richard Cliff, Jonathan Rose, Altera and the University of Toronto
	9:10	*HARP: Hardwired Routing Pattern FPGAs* Satish Sivaswamy, Gang Wang, Cristinel Ababei, Kia Bazargan, Ryan Kastner, Eli Bozorgzadeh, University of Minnesota, University of California
9:30am-10:30am	Poster Session 1: New CAD Techniques and Methods Chair: Jason Cong, UCLA Coffee Break	

10:30am-11:30am	Session 2: Advances in FPGA CAD Chair: Jonathan Rose, University of Toronto	
	10:30	*Skew-programmable clock design for FPGA and skew-aware placement* Chao-Yang Yeh, Malgorzata Marek-Sadowska, University of California - Santa Barbara
	10:50	*The Effect of Post-Placement Pin Permutation on Timing* Yuzheng Ding, Peter Suaris, Nanchi Chou, Mentor Graphics
	11:10	*Simultaneous Timing-Driven Placement and Duplication* Gang Chen, Jason Cong, Magma Design Automation, University of California at Los Angeles
12:00-1:30pm	Lunch	
1:30pm-2:30pm	Session 3: Computation Algorithms for FPGAs Chair: Tom Kean, Algotronix	
	1:30	*Sparse Matrix-Vector Multiplication on FPGAs* Ling Zhuo and Viktor K. Prasanna, University of Southern California
	1:50	*Floating Point Sparse Matrix-Vector Multiply for FPGAs* Michael deLorimier, André DeHon, California Institute of Technology
	2:10	*64-bit Floating-Point FPGA Matrix Multiplication* Yong Dou, S. Vassiliadis, G.K. Kuzmanov, G.N. Gaydadjiev, National Laboratory for Parallel and Distributed Processing and Delft University of Technology
2:30pm-3:30pm	Poster Session 2: FPGA Architectures and Circuits Chair: Guy Lemieux, University of British Columbia Coffee Break	

3:30pm-4:30pm	Session 4: Computation Techniques for FPGAs Chair: John Wawrzynek, UC Berkely	
	3:30	*Instruction Set Extension with Shadow Registers for Configurable Processors* Jason Cong, Yiping Fan, Guoling Han, Glenn Reinman, Zhiru Zhang, University of California at Los Angeles
	3:50	*An FPGA-based VLIW Processor with Custom Hardware Execution* Alex K. Jones, Raymond Hoare, Dara Kusic, Joshua Fazekas, John Foster, University of Pittsburgh
	4:10	*Techniques for Synthesizing Binaries to an Advanced Register/Memory Structure* Greg Stitt, Zhi Guo, Frank Vahid, Walid Najjar, University of California - Riverside
6:00pm-7:00pm	Conference Banquet	
7:00pm-10:00pm	Panel Session: FPGA Startups: Diamonds or Dust? Chairs: Guy Lemieux and John Lockwood	

Tuesday, February 22		
7:00am-5:00pm	Registration	
7:30am-8:15am	Continental Breakfast	
8:00am-5:00pm	Sponsor and Exhibit Room	
8:30am-9:30am	Session 5: New Directions for Programmable Devices Chair: Steve Trimberger, Xilinx	
	8:30	*Design of Programmable Interconnect for Sublithographic Programmable Logic Arrays* André DeHon, California Institute of Technology
	8:50	*Analysis of Yield Loss due to Random Photolithographic Defects in the Interconnect Structure of FPGAs* Nicola Campregher, Peter Y.K. Cheung, George A. Constantinides, Milan Vasilko, Imperial College
	9:10	*Soft Error Rate Estimation and Mitigation for SRAM-Based FPGAs* Ghazanfar Asadi and Mehdi B. Tahoori, Northeastern University
9:30am-10:30am	Poster Session 3: Novel Applications of Reconfigurability Chair: Scott Hauck, University of Washington Coffee Break	

10:30am-11:30am	Session 6: Synthesis and Timing Analysis for FPGAs Chair: Eric Sather, Actel	
	10:30	*Automated Synthesis for Asynchronous FPGAs* Song Peng, David Fang, John Teifel, and Rajit Manohar, Cornell University
	10:50	*Efficient Static Timing Analysis And Applications Using Edge Masks* Mike Hutton, David Karchmer and Bryan Archell, Altera
	11:10	*Evaluating Heuristics in Automatically Mapping Multi-Looped Applications to FPGAs* Heidi Ziegler and Mary Hall, University of Southern California
12:00-1:30pm	Lunch	
1:30pm-2:30pm	Session 7: FPGA Circuit Design and Layout Chair: Vaughn Betz, Altera	
	1:30	*Circuits and Architectures for Vdd Programmable FPGAs* Yan Lin, Fei Li and Lei He, University of California, Los Angeles
	1:50	*Combining Low-Leakage Techniques for FPGA design* Andrea Lodi, Luca Ciccarelli, Roberto Giansante, University of Bologna
	2:10	*Design, Layout and Verification of an FPGA using Automated Tools* Ian Kuon, Aaron Egier and Jonathan Rose, University of Toronto
2:30pm-3:30pm	Coffee Break	
3:30pm-4:30pm	Session 8: Novel FPGA Applications Chair: Katherine Compton, UW-Madison	
	3:30	*Hyper Customized Processors for Bio-Sequence Database Scanning on FPGAs* Tim Oliver, Bertil Schmidt and Douglas Maskell, Nanyang Technological University
	3:50	*Efficient Packet Classification for Network Intrusion Detection using FPGA* Haoyu Song, John W. Lockwood, Washington University
	4:10	*CUSP: A Modular Framework for High Speed Network Applications on FPGAs* Graham Schelle and Dirk Grunwald, University of Colorado at Boulder
4:30pm-4:40pm	Closing Remarks: Herman Schmit, Steve Wilton	

Poster Session 1: New CAD Techniques and Methods

A Petri-Net Based Pre-Runtime Scheduler for Dynamically Self-Reconfiguration of FPGAs
Remy Eskinazi, Manoel E. de Lima, Paulo R. M. Maciel, Carlos A.Valderrama, Abel G. Filho, and Paulo S.B. Nascimento

Figaro: An Automatic Tool Flow for Designs with Dynamic Reconfiguration
Kelly Nasi, Martin Daněk, Theodoros Karoubalis, and Zdeněk Pohl

A New Universal Test Pattern Auto-generating Approach for FPGA Logic Resources
Yirong OuYang, and Jiarong Tong

3D FPGAs: Placement, Routing, and Architecture Evaluation
Cristinel Ababei, Hushrav Mogal, and Kia Bazargan

VPart: An Automatic Partitioning Tool for Dynamic Reconfiguration
Leos Kafka, Rafal Kielbik, Rudolf Matousek, and Juan Manuel Moreno

Efficient Utilization of Heterogeneous Routing Resources for FPGAs
Deepak Rautela and Rajendra Katti

Enabling a RealTime Solution for Neuron Detection with Reconfigurable Hardware
Ben Cordes, Jennifer Dy, Miriam Leeser, and James Goebel

Efficient Methodology for Detection and Correction of SEU-based Interconnect Errors in FPGAs using Partial Reconfiguration
E. Syam Sundar Reddy, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti, and Vijaykrishnan Narayanan

Time-multiplexed Execution on the Dynamically Reconfigurable Processor - A Performance/Cost Evaluation
Yohei Hasegawa, Shohei Abe, Katsuaki Deguchi, Masayasu Suzuki, and Hideharu Amano

Architecture Adaptive Routability-Driven Placement for FPGAs
Akshay Sharma, Carl Ebeling, and Scott Hauck

Routing Algorithms: Enhancing Routability and Enabling ECO
Taraneh Taghavi, Soheil Ghiasi, and Majid Sarrafzadeh

A Leakage-Aware CAD Flow for MTCMOS FPGA Architectures
H. Hassan, M. Anis, and M. Elmasry

An Execution Environment For Reconfigurable Computing
W. Fu and K. Compton

Poster Session 2: FPGA Architectures and Circuits

Energy-efficient FPGA interconnect architecture design
Rohini Krishnan, R.I.M.P. Meijer, and Durand Guillaume

Exploration of Heterogeneous Reconfigurable Architectures
Alastair M. Smith, George A. Constantinides and Peter Y. K. Cheung

Domain Specific Non-Uniform Routing Architecture for Embedded Programmable IP Core
Wen Yujie, Tong Jiarong, and Charles Chiang

Prototyping Globally Asynchronous Locally Synchronous Circuits on Commercial Synchronous FPGAs
Mehrdad Najibi, Kamran Saleh, Mohsen Naderi, Hossein Pedram and Mehdi Sedighi

3D-SoftChip: A Novel 3D Vertically Integrated Adaptive Computing System
Chul Kim, Alex Rassau, and Mike Myung-Ok Lee

Dynamic Hardware Multiplexing for Coarse Grain Reconfigurable Architectures
Pascal Benoit, Lionel Torres, Gilles Sassatelli, Michel Robert, and Gaston Cambon

Soft Multiprocessor Systems for Network Applications
Yujia Jin, William Plishker, Kaushik Ravindran, Nadathur Satish and Kurt Keutzer

Firm-core Virtual FPGA for Just-in-Time FPGA Compilation
Roman Lysecky, Kris Miller, Frank Vahid, and Kees Vissers

Hierarchical LUT Structures for Leakage Power Reduction
Somsubhra Mondal, Seda Ogrenci Memik, and Debasish Das

Dual-Vt FPGA Design for Leakage Power Reduction
Akhilesh Kumar, and Mohab Anis

SMPS: An FPGA-based Prototyping Environment for Multiprocessor Embedded Systems
Ankit Mathur, Mayank Agarwal, Soumyadeb Mitra, Anup Gangwar, M. Balakrishnan, and Subhashis Banerjee

Poster Session 3: Novel Applications of Reconfigurability

Configurable Hardware Solutions for Computing Autocorrelation Coefficients: a Case Study
J. E. Rice, K.B. Kent, T. Ronda and Z. Yong

Dynamic Reconfiguration in FPGA-based SoC Designs
Roman Bartosinski , Martin Daněk, Petr Honzík, and Rudolf Matoušek

A Partial Reconfigurable FPGA Implementation for Industrial Controllers Using SFC-Petri net Description

Paulo Sérgio, B. Nascimento, Paulo Romero M. Maciel, Manoel E. Lima, Remy E. Sant'ana, Abel Guilhermino, and S. Filho

Design and Implementation of Packet Classification with FPGA

Wang Yong-gang and Yan Tian-xin

Image Processing Library for Reconfigurable Computers

Mohamed Taher, Esam El-Araby, Tarek El-Ghazawi, and Kris Gaj

A 2005 Review of FPGA Arithmetic

Stéphane Simard, Rachid Beguenane, Éric Larouche, and Luc Morin

Rapid Prototyping of a Test Harness for Forward Error Correcting Codes

Edward Brown, James Irvine, and Bill Wilkie

A Framework for Rule Processing in Reconfigurable Network Systems

Michael E. Attig and John W. Lockwood

An FPGA Based SDRAM Controller with Complex QoS Scheduling and Traffic Shaping

Sven Heithecker and Rolf Ernst

An Integrated Framework for the High Level Design of High Performance Signal Processing Circuits on FPGAs

K. Benkrid and S.Belkacemi

A VLIW-Based CryptoProcessor on FPGAs Architecture and Performance Issues

Edward David Moreno, Fábio Dacêncio Pereira, and Rodolfo B. Chiaramonte

Reconfigurable Computers: An Empirical Analysis

Tarek El-Ghazawi, Kris Gaj, Nikitas Alexandridis, Allen Michalski, Devrim Fidanci, Mohamed Taher, Esam El-Araby, Esmail Chitalwala, and Proshanta Saha

Choice of Base Revisited: Higher Radices for FPGA-based Floating-Point Computation

Bryan C. Catanzaro, and Brent E. Nelson

Accelerating Mutual Information-based 3D Medical Image Registration with An FPGA Computing Platform

Jianchun Li, Christos Papachristou, and Raj Shekhar

An FPGA Generator for Multipoint Distributed Random Variables

Nicola Bruti Liberati, Eckhard Platen, Filippo Martini, and Massimo Piccardi

A Constant Array Multiplier Core Generator with Dynamic Partial Evaluation Architecture Selection

Bo Yang, Nikhil Joshi, and Ramesh Karri