



FPGA 2004 Advance Program

ACM/SIGDA Eleventh International Symposium on Field Programmable Gate Arrays

Sponsored by ACM/SIGDA
with support from Actel, Altera and Xilinx
Monterey Beach Hotel, Monterey, California
February 22-24, 2004
<http://fpga2004.ece.ubc.ca/>

* Pre-register by January 22, 2004

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Join us at the beach in Monterey, California for the eleventh ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA2004), the premier forum for novel work in all areas related to FPGA technology. This year's FPGA Symposium features twenty-four papers describing cutting-edge FPGA work. Authors present novel work on FPGA architecture from commercial vendors, research labs and universities. Innovative software research highlights high-speed and high-quality FPGA design. Papers also describe novel devices and software for reconfigurable computing. Finally, FPGA 2004 showcases some impressive applications of FPGAs.

FPGA2004 provides a relaxed environment for informal information exchange, networking and stimulating discussions with the leaders in FPGA research and development from academia and industry. Paper sessions are separated by ample time to peruse the poster presentations and discuss the latest-breaking FPGA news. This year, FPGA 2004 will be held at the Monterey Beach Hotel, a stunning setting guaranteed to facilitate informal discussion as well as formal presentations.

The FPGA 2004 dinner banquet will be followed by a panel discussion. This is an opportunity not to be missed.

If you are at all interested in FPGA technology and developments, you won't want to miss this event.

Organizing Committee

General Chair	Russ Tessier, University of Massachusetts - Amherst
Program Chair	Herman Schmit, Everychip
Publicity Chair	Steve Wilton, University of British Columbia
Panel Chair	André DeHon, Caltech
Finance Chair	Martine Schlag, University of California, Santa Cruz

Program Committee

Ray Andraka, Andraka Consulting	Michael Butts, Cadence	Vaughn Betz, Altera
Jason Cong, UCLA	John Costello, Altera	Andre DeHon, Caltech
Eugene Ding, Mentor Graphics	James Hoe, CMU	Rajeev Jayaraman, Xilinx
Tom Kean, Algotronix	Arun Kundu, Actel	John Lockwood, Wash U
Margaret Marek-Sadowska, UCSB	Herman Schmit, CMU	Satwant Singh, Lattice
Russ Tessier, U. Mass.-Amherst	Steve Trimberger, Xilinx	John Wawrzynek, UCB
Steve Wilton, U. British Columbia	Micheal Wirthlin, BYU	Martin Wong, U. Texas

PROGRAM

Sunday, February 22, 2004

6:00PM	Registration
7:00PM	Welcoming Reception

Monday, February 23, 2004

7:30 AM	Continental Breakfast and Registration
8:20 AM	Opening Remarks , Russ Tessier, Herman Schmit

Session 1. Architectures

Chair: TBD

8:30 AM	The SFRA: A Corner-Turn FPGA Architecture , N. Weaver, J. Hauser, J. Wawrzynek, University of California at Berkeley
8:50 AM	Exploration of Pipelined FPGA Interconnect Structures , A. Sharma, K. Compton, C. Ebeling, S. Hauck, University of Washington
9:10 AM	Evaluation of Low-Leakage Design Techniques for Field Programmable Gate Arrays , A. Rahman, Polavarapuv, Polytechnic University
9:30 AM	Coffee Break and Poster Presentations

Session 2. Tools and Architectures for Power Minimization

Chair: TBD

10:30 AM	Active Leakage Power Optimization for FPGAs , J. Anderson, F. Najm, T. Tuan, University of Toronto / Xilinx
10:50 AM	Low-power FPGA using Dual-Vdd/Dual-Vt Techniques , Fei Li, Yan Lin, Lei He and Jason Cong, UCLA
11:10 AM	Reducing Leakage Energy in FPGAs Using Region-Constrained Placement , A. Gayasen, Y. Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, T. Tuan, Penn State / Xilinx
11:30 AM	Poster Presentations

12:00 N	Lunch
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Session 3. Applications I

Chair: TBD

1:30 PM	A High Performance 32-bit ALU for Programmable Logic , P. Metzgen, Altera
1:50 PM	An Embedded True Random Number Generator for Field Programmable Gate Arrays , P. Kohlbrenner, K. Gaj, George Mason University
2:10 PM	Making Visible the Thermal Behaviour of Embedded Microprocessors on FPGAs , S. Lopez-Buedo, E Boemo, Universidad Autonoma de Madrid
2:30 PM	Poster Presentations

Session 4. Tools

Chair: TBD

3:30 PM	A Synthesis-Oriented Omniscient Manual Editor , T. Czajkowski, J. Rose, University of Toronto
3:50 PM	Incremental Physical Resynthesis for Timing Optimization , P. Suaris, L. Liu, Y. Ding, N. Chou, Mentor Graphics
4:10 PM	Low Power Technology Mapping for FPGA Architectures with Dual Supply Voltages , Deming Chen, Jason Cong, Fei Li, Lei He, UCLA
4:30 PM	Poster Presentations

6:00 PM	Dinner
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7:00 PM - 10:00 PM	<p>Panel - FPGA Tools: Hand-me-downs or Tailor-made?</p> <p>Traditionally, FPGAs have been the bastard step-brother of ASICs. They've been forced to act-like ASICs and fit themselves into the ASIC development model to be accepted into society. This has meant ignoring their unique strengths (e.g. reprogrammability, late-binding and run-time reconfiguration). Today, however, FPGAs are becoming more socially acceptable for their own merits; the majority of new design starts are FPGA designs. As FPGAs rise from under the shadow of their aging brother, should they continue to try to wear his hand-me-downs? Or is it time to develop more suitable models that lets them shine? At the same time, the old ASIC model is not even serving ASICs well, and new models for developing ASICs are emerging. All this may encourage us to rethink how we should be programming FPGA-based systems.</p> <ul style="list-style-type: none"> ▪ Use the traditional, ASIC model --- it's tried and true, has demonstrated success ▪ Use the traditional, sequential processor model --- Compile programs from C down to FPGAs...perhaps evolving FPGAs to better support ▪ Use the emerging C-level design ▪ Use concurrent and/or streaming models (incl. CSP, Matlab/simulink, Ptolemy, SCORE, Stream-C) ▪ Use a biologically inspired model (neural networks, genetic programming...) <p>Moderator: Brad Hutchings (BYU, Everychip)</p> <p>Panelist List: Andre' DeHon (Caltech) Daryl Rudusky (Celoxica) James Hwang (Xilinx) Nikhil (BlueSpec) Salil Raje (Hier Design) Adrian Stoica (JPL)</p>
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Tuesday, February 24, 2004

7:30 AM	Breakfast
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Session 5. Logic Novel Devices and Approaches to Programmable Devices

Chair: TBD

8:30 AM	Nanowire-Based Sublithographic Programmable Logic Arrays , A. DeHon, M. Wilson, Caltech
8:50 AM	Highly Pipelined Asynchronous FPGAs , J. Teifel, R. Manohar, Cornell
9:10 AM	A Magnetoelectronic Macrocell Employing Reconfigurable Threshold Logic , S. Ferrera, N. Carter, University of Illinois
9:30 AM	Coffee Break and Poster Presentations

Session 6. Reconfigurable Computing: Analysis and Trends

Chair: TBD

10:30 AM	Flexibility Measurement of Domain-Specific Reconfigurable Hardware , K. Compton, S. Hauck, University of Wisconsin / University of Washington
10:50 AM	A Quantitative Analysis of the Speedup Factors of FPGAs over Processors , Z. Guo, W. Najjar, F. Vahid, K. Vissers, UC Riverside / UC Berkeley
11:10 AM	FPGAs vs. CPUs: Trends in Peak Floating-Point Performance , K. Underwood, Sandia Labs
	Poster Presentations

12:00 N	Lunch
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Session 7. **Reconfigurable Computing: Architectures and Applications**

Chair: TBD

1:30 PM	Application Specific Instruction Generation for Reconfigurable Systems , J. Cong, Y. Fan, G. Han, Z. Zhang, UCLA
1:50 PM	Using Reconfigurability to Achieve RealTime Profiling for Hardware/Software Codesign , L. Shannon, P. Chow, University of Toronto
2:10 PM	A Reconfigurable Unit for a Clustered Programmable-Reconfigurable Processor , R. Kujoth, C.-W.Wang, D. Gottlieb, J. Cook, N. Carter, University of Illinois
2:30 PM	Coffee Break and Poster Presentations

Session 8. **Applications II**

Chair: TBD

3:30 PM	An FPGA Implementation of the Two-Dimensional Finite-Difference Time-Domain (FDTD) Algorithm , W. Chen, P. Kosmas, M. Leeser, C. Rappaport, Northeastern University
3:50 PM	Time and Area Efficient Pattern Matching on FPGAs , Z. Baker, V. Prasanna, USC
4:10 PM	A Compiled Accelerator for Biological Cell Signaling Simulations , J. Keane, C. Bradley, C. Ebeling, University of Washington
4:30 PM	Closing Remarks , Russ Tessier, Herman Schmit

Hotel Reservations

FPGA 2004 will be held at the Monterey Beach Resort. Attendees who will be staying at the hotel must make hotel reservations in addition to their conference registration. To make reservations at the hotel, contact:

The Beach Resort
2600 Sand Dunes Drive
Monterey, CA 93940
USA+831-394-3321

<http://www.montereybeachresort.com>

Tell them that you are with the **ACM/FPGA** conference to get the conference rate of \$112 Gardenside or \$152 Oceanside. The room rate is the same for single or double. The conference cut off-date is January 29, 2004. Reservations received after January 29 will be accepted on a space and rate available basis only.

For information on the Monterey area, visit the Web site: <http://www.gomonterey.com/>

REGISTRATION FORM FOR FPGA'04
ACM/SIGDA International Symposium on Field Programmable Gate Arrays
February 22-24, 2004 Monterey, California, USA
To register on the web, go to <http://www.regmaster.com/fpga2004.html>

Name (first, middle, last): _____

Affiliation (for badge): _____

Title/Job Function: _____

Address: _____

City: _____ State: _____ Zip Code: _____

Country: _____ Email: _____

Phone: (____) _____ Fax: (____) _____

ACM/SIG Member ID: _____ Student ID: _____

Special Needs: _____ Special Dietary Requirements: Vegetarian Kosher Vegan

Do not include my name, address and e-mail id in the conference attendee listing _____.

PLEASE NOTE: Conference registration fee includes one copy of the conference proceedings, 2 continental breakfasts, 2 lunches, one ticket to Sunday's Reception and one ticket to Monday's Dinner.

REGISTRATION FEES (Please circle appropriate fees)

The cut off date for preregistration is February 11, 2004. After this date you must register on-site.

	Registration on or Before 1/21/04			Registration after 1/21/04		
	<i>Member</i>	<i>Non-Member</i>	<i>Student</i>	<i>Member</i>	<i>Non-Member</i>	<i>Student</i>
FPGA'04 Conference	\$325.00	\$425.00	\$ 85.00	\$400.00	\$500.00	\$ 95.00

Extras:

Guest *Monday Dinner* Tickets: ____ tickets x \$60 = _____

Total Fees: US \$ _____ (Make checks payable to ACM/FPGA'04 Conference)

Payment included (circle one): American Express Master Card Visa Check

Credit Card Number: _____ Expiration Date: _____

Names as it appears on Credit Card: _____

Signature: _____

For questions (8:30 am - 4:30 PM EST), Email: acmhelp@acm.org Telephone: (US and Canada) 1-800-342-6626, (outside the US) 1-212-626-0500. For Credit Card payments, Fax 1-212-944-1318,. **If paying by check, mail check with registration form to:**

ACM Member Services, P.O. Box 11405, New York, NY 10286-1405, USA

Cancellations must be received in writing by contacting the ACM Member Services Department. A US \$50 cancellation fee will be charged. **You should receive e-mail confirmation within 3 business days. If you do not please contact our member services department at the above contact information.**

Remember, if you are planning to stay at the conference hotel, you must ALSO make a hotel room reservation: USA+831-394-3321 <http://www.montereybeachresort.com/>