FPGA 2001 Final Program

2001 ACM/SIGDA Ninth International Symposium on Field Programmable Gate Arrays
Doubletree Hotel, Monterey, California
February 11-13, 2001
Sponsored by ACM/SIGDA
with support from Altera, Xilinx, Agere Systems, Cypress and Actel

Sunday, February 11, 2001

6:00PM Registration

7:00PM Welcoming Reception

Monday, February 12, 2001

7:30AM Continental Breakfast and Registration

8:20AM Opening remarks: Scott Hauck, Martine Schlag

Session 1. **Placement and Routing**

Chair: Carl Ebeling, *University of Washington*

8:30AM **Timing-Driven Placement for Hierarchical Programmable Logic Devices.**
Michael Hutton, Khosrow Adibasmii and Andrew Leaver, *Altera.*

8:50AM **LRoute: A Delay Minimal Router for Hierarchical CPLDs.**
K.K. Lee, *Synopsys,* Martin D.F. Wong, *University of Texas at Austin.*

9:10AM **A Crosstalk-Aware Timing-Driven Router for FPGAs.**
Steven J.E. Wilton, *University of British Columbia.*

9:30AM **Runtime and Quality Tradeoffs in FPGA Placement and Routing.**
Chandra Mulpuri and Scott Hauck, *University of Washington.*

9:50AM Coffee Break and Poster Presentations.

Session 2. **Technology Mapping**

Chair: Steven Wilton, *University of British Columbia*

10:50AM **Performance-Driven Mapping for CPLD Architectures.**
Deming Chen, Jason Cong, Milos Ercegovac and Zhijun Huang,
University of California, Los Angeles.

11:10AM **Simultaneous Logic Decomposition with Technology Mapping in FPGA Designs.**
Gang Chen and Jason Cong, *University of California, Los Angeles.*

11:30AM Poster Presentations

12:00PM Lunch

Session 3. **Routing Architectures**

Chair: Tom Kean, *Algotronix*

1:30PM **Using Sparse Crossbars within LUT Clusters.**
Guy G. Lemieux and David M. Lewis, *University of Toronto.*

1:50PM **Detailed Routing Architectures for Embedded Programmable Logic IP Cores.**
Peter Hallschmid and Steven J.E. Wilton, *University of British Columbia.*

2:10PM **Mixing Buffers and Pass Transistors in FPGA Routing Architectures.**
Mike Sheng and Jonathan Rose, *University of Toronto.*

2:30PM Coffee Break and Poster Presentations.

Session 4. **Applications**

Chair: Ray Andraka, *Andraka Consulting*

3:30PM **Reprogrammable Network Packet Processing on the Field Programmable Port Extender (FPX)**. John W. Lockwood, Naji Naufel, Jon S. Turner and David E. Taylor, *Washington University*.

3:50PM **Fast Implementations of Secret-Key Block Ciphers Using Mixed Inner- and Outer-Round Pipelining.** Pawel Chodowiec, Po Khuon, and Kris Gaj, *George Mason University.*

4:10PM **Algorithmic Transformations in the Implementation of K-means Clustering on Reconfigurable Hardware.** Mike Estlick, Miriam Leeser, *Northeastern University*; John J. Szymanski, James Theiler, *Los Alamos National Laboratory.*

6:00PM Dinner

7:30PM **Is marriage in the cards for programmable logic, microprocessors and ASICs?**

Moderator: Sinan Kaptanoglu*, Adaptive Silicon*
Panelists: John East, *Actel*
Tim Garverick, *Adaptive Silicon*
Scott Hauck, *University of Washington*
David Papworth, *Intel*
Danesh Tavana, *Triscend*
Steve Trimberger, *Xilinx*
Ronnie Vasishta, *LSI Logic*

The panelists focus on the possibility, likelihood or inevitability of combinations of programmable logic, microprocessors and ASICs in a single chip. Will they be as general as possible or application specific? Will all three types of logic be involved or perhaps only two? How much of the die area should be allocated to programmable logic? How will the CAD tools cope with the speed mismatch between the programmable logic and fixed logic on the same chip? How will the designs be partitioned into programmable and parts; will it be done by humans or by CAD tools? These future predictions may depend on the system design size. Are the answers for 500K gate system designs different from those for 5,000K gate system designs? What will happen when 50,000K gate system designs become commonplace in 5 years?

Tuesday, February 13, 2001

7:30AM Continental Breakfast and Registration

Session 5. **Reconfigurable Computing**

Chair: Steve Trimberger, *Xilinx*

8:30AM **Attacking the Semantic Gap Between Application Programming Languages and Configurable Hardware.**
Greg Snider, Barry Shackleford and Richard J. Carter, *Hewlett-Packard Laboratories*.

8:50AM **Matching and Searching Analysis for Parallel Hardware Implementation on FPGAs.**
Pablo Moisset, Pedro Diniz and Joonseok Park*,*
University of Southern California/Information Sciences Institute.

9:10AM **Evaluation of the Streams-C C-to-FPGA Compiler: An Applications Perspective.**
Janette Frigo, Maya Gokhale, *Los Alamos National Laboratory,*
and Dominique Lavenier, *IRISA-CNRS*.

9:30AM **The Effect of Reconfigurable Units in Superscalar Processors.**
Jorge E. Carrillo E. and Paul Chow, *University of Toronto*.

9:50AM Coffee Break and Poster Presentations.

Session 6. **Pipelined Routing Architectures**

Chair: Andre DeHon, *Cal Tech*

10:50AM **Interconnect Pipelining in a Throughput-Intensive FPGA Architecture.**
Amit Singh, Arindam Mukherjee and Malgorzata Marek-Sadowska,
University of California, Santa Barbara.

11:10AM **The Case for Registered Routing Switches in Field Programmable Gate Arrays.**
Deshanand P. Singh and Stephen D. Brown. *University of Toronto.*

11:30AM Poster Presentations.

12:00PM Lunch

Session 7. **Issues in FPGA-based Systems**

Chair: Chuck Stroud, *University of North Carolina - Charlotte*

1:30PM **Configuration Compression for FPGA-based Embedded Systems.**
Andreas Dandalis and Viktor K. Prasanna, *University of Southern California.*

1:50PM **A Memory Coherence Technique for Online Transient Error Recovery of FPGA Configurations.**
Wei-Je Huang and Edward J. McCluskey, *Stanford University.*

2:10PM **Run-Time Defect Tolerance using JBits.**
Prasanna Sundararajan and Steven A. Guccione, *Xilinx.*

2:30PM Coffee Break and Poster Presentations.

Session 8**. Applications in Image/Video Compression**

Chair: Miriam Leeser, *Northeastern University*

3:30PM **A Pipelined Architecture for Partitioned DWT Based Lossy Image Compression using FPGA's.**
Jörg Ritter and Paul Molitor, *Martin-Luther-University Halle-Wittenberg.*

3:50PM **An FPGA-Based Video Compressor for H.263 Compatible Bit Streams.**
G. Lienhart, R. Männer, *University of Mannheim*, R. Lay and K.H. Noffz, *Silicon Software GmbH*

4:10PM **FPGA Implementation of a Novel, Fast Motion Estimation Algorithm for Real-Time Video Compression.** S. Ramachandran and S. Srinivasan, *Indian Institute of Technology, Madras*

4:30PM Closing Remarks: Scott Hauck, Martine Schlag

Organizing Committee

General Chair:	Scott Hauck, U. Washington
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Publicity Chair:	Russ Tessier, U. Mass.–Amherst
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