Poster Session 1: New CAD Techniques and Methods

A Petri-Net Based Pre-Runtime Scheduler for Dynamically Self-Reconfiguration of FPGAs

Figaro: An Automatic Tool Flow for Designs with Dynamic Reconfiguration
Kelly Nasi, Martin Daněk, Theodoros Karoubalis, and Zdeněk Pohl

A New Universal Test Pattern Auto-generating Approach for FPGA Logic Resources
Yirong OuYang, and Jiarong Tong

3D FPGAs: Placement, Routing, and Architecture Evaluation
Cristinel Ababei, Hushrav Mogal, and Kia Bazargan

VPart: An Automatic Partitioning Tool for Dynamic Reconfiguration
Leos Kafka, Rafal Kielbik, Rudolf Matousek, and Juan Manuel Moreno

Efficient Utilization of Heterogeneous Routing Resources for FPGAs
Deepak Rautela and Rajendra Katti

Enabling a RealTime Solution for Neuron Detection with Reconfigurable Hardware
Ben Cordes, Jennifer Dy, Miriam Leeser, and James Goebel

Efficient Methodology for Detection and Correction of SEU-based Interconnect Errors in FPGAs using Partial Reconfiguration
E. Syam Sundar Reddy, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti, and Vijaykrishnan Narayanan

Yohei Hasegawa, Shohei Abe, Katsuaki Deguchi, Masayasu Suzuki, and Hideharu Amano

Architecture Adaptive Routability-Driven Placement for FPGAs
Akshay Sharma, Carl Ebeling, and Scott Hauck

Routing Algorithms: Enhancing Routability and Enabling ECO
Taraneh Taghavi, Soheil Ghiasi, and Majid Sarrafzadeh

A Leakage-Aware CAD Flow for MTCMOS FPGA Architectures
H. Hassan, M. Anis, and M. Elmasry

An Execution Environment For Reconfigurable Computing
W. Fu and K. Compton
Poster Session 2: FPGA Architectures and Circuits

Energy-efficient FPGA interconnect architecture design
Rohini Krishnan, R.I.M.P. Meijer, and Durand Guillaume

Exploration of Heterogeneous Reconfigurable Architectures
Alastair M. Smith, George A. Constantinides and Peter Y. K. Cheung

Domain Specific Non-Uniform Routing Architecture for Embedded Programmable IP Core
Wen Yujie, Tong Jiarong, and Charles Chiang

Prototyping Globally Asynchronous Locally Synchronous Circuits on Commercial Synchronous FPGAs
Mehrdad Najibi, Kamran Saleh, Mohsen Naderi, Hossein Pedram and Mehdi Sedighi

Chul Kim, Alex Rassau, and Mike Myung-Ok Lee

Dynamic Hardware Multiplexing for Coarse Grain Reconfigurable Architectures
Pascal Benoit, Lionel Torres, Gilles Sassatelli, Michel Robert, and Gaston Cambon

Soft Multiprocessor Systems for Network Applications
Yujia Jin, William Plishker, Kaushik Ravindran, Nadathur Satish and Kurt Keutzer

Firm-core Virtual FPGA for Just-in-Time FPGA Compilation
Roman Lysecky, Kris Miller, Frank Vahid, and Kees Vissers

Hierarchical LUT Structures for Leakage Power Reduction
Somsubhra Mondal, Seda Ogrenci Memik, and Debasish Das

Dual-Vt FPGA Design for Leakage Power Reduction
Akhilesh Kumar, and Mohab Anis

SMPS: An FPGA-based Prototyping Environment for Multiprocessor Embedded Systems
Ankit Mathur, Mayank Agarwal, Soumyadeb Mitra, Anup Gangwar, M. Balakrishnan, and Subhashis Banerjee

Poster Session 3: Novel Applications of Reconfigurability

Configurable Hardware Solutions for Computing Autocorrelation Coefficients: a Case Study
J. E. Rice, K.B. Kent, T. Ronda and Z. Yong

Dynamic Reconfiguration in FPGA-based SoC Designs
Roman Bartosinski, Martin Daněk, Petr Honzík, and Rudolf Matoušek
A Partial Reconfigurable FPGA Implementation for Industrial Controllers Using SFC-Petri net
Description
Paulo Sérgio, B. Nascimento, Paulo Romero M. Maciel, Manoel E. Lima, Remy E. Sant’ana, Abel Guilhermino, and S. Filho

Design and Implementation of Packet Classification with FPGA
Wang Yong-gang and Yan Tian-xin

Image Processing Library for Reconfigurable Computers
Mohamed Taher, Esam El-Araby, Tarek El-Ghazawi, and Kris Gaj

A 2005 Review of FPGA Arithmetic
Stéphane Simard, Rachid Beguenane, Éric Larouche, and Luc Morin

Rapid Prototyping of a Test Harness for Forward Error Correcting Codes
Edward Brown, James Irvine, and Bill Wilkie

A Framework for Rule Processing in Reconfigurable Network Systems
Michael E. Attig and John W. Lockwood

An FPGA Based SDRAM Controller with Complex QoS Scheduling and Traffic Shaping
Sven Heithecker and Rolf Ernst

An Integrated Framework for the High Level Design of High Performance Signal Processing Circuits on FPGAs
K. Benkrid and S.Belkacemi

A VLIW-Based CryptoProcessor on FPGAs Architecture and Performance Issues
Edward David Moreno, Fábio Dacêncio Pereira, and Rodolfo B. Chiaramonte

Reconfigurable Computers: An Empirical Analysis
Tarek El-Ghazawi, Kris Gaj, Nikitas Alexandridis, Allen Michalski, Devrim Fidanci, Mohamed Taher, Esam El-Araby, Esmail Chitalwala, and Proshanta Saha

Choice of Base Revisited: Higher Radices for FPGA-based Floating-Point Computation
Bryan C. Catanzaro, and Brent E. Nelson

Accelerating Mutual Information-based 3D Medical Image Registration with An FPGA Computing Platform
Jianchun Li, Christos Papachristou, and Raj Shekhar

An FPGA Generator for Multipoint Distributed Random Variables
Nicola Bruti Liberati, Eckhard Platen, Filippo Martini, and Massimo Picardi

A Constant Array Multiplier Core Generator with Dynamic Partial Evaluation Architecture Selection
Bo Yang, Nikhil Joshi, and Ramesh Karri